

THE INVENTION CLAIMED IS:

1 1. A test control device adapted to:
2 couple to an electronic device that is adapted to be partitioned into
3 segments by using clock gating or signal gating; and
4 control the electronic device to identify one of the segments that is
5 a source of a failure by selectively disabling at least one of the segments.

1 2. A computer system chip comprising:
2 a test control device adapted to:
3 couple to an electronic device to be tested;
4 partition the electronic device into a plurality of segments
5 by using clock gating or signal gating; and
6 control the electronic device to identify one of the plurality
7 of segments that is a source of a failure by selectively disabling at least one of the
8 plurality of segments.

1 3. The computer system chip of claim 2 wherein the test control
2 device is adapted to partition the electronic device into the plurality of segments by using
3 clock gating.

1 4. The computer system chip of claim 2 wherein the test control
2 device is adapted to partition the electronic device into the plurality of segments by using
3 signal gating.

1 5. A computer system chip comprising:
2 a plurality of functional units;

a plurality of clock control macros, each clock control macro coupled to a different one of the plurality of functional units and adapted to generate a system clock for the functional unit to which the clock control macro is coupled; and a register coupled to the plurality of clock control macros, and adapted to:

partition the computer system chip into a plurality of segments by using clock gating or signal gating; and control the computer system chip to identify one of the plurality of segments that is a source of a failure by selectively disabling at least one of the plurality of segments.

6. The computer system chip of claim 5 wherein the register is adapted to partition the computer system chip into the plurality of segments by using clock gating.

7. The computer system chip of claim 5 wherein the register is adapted to partition the computer system chip into the plurality of segments by using signal gating.

8. The computer system chip of claim 5 wherein the register is further adapted to apply a bit to at least one of the clock control macros; and wherein the at least one clock control macro is adapted to employ the bit to stop or gate-off a system clock provided to the functional unit coupled to the at least one clock control macro.

1 9. The computer system chip of claim 5 wherein the plurality of
2 functional units include at least one of an L1 cache array, an L1 directory array, an
3 instruction unit and an execution unit.

1 10. The computer system chip of claim 5 wherein the plurality of clock
2 control macros are clock gates.

1 11. A testing arrangement comprising:
2 a test control device adapted to:
3 couple to an electronic device that is adapted to be
4 partitioned into segments by using clock gating or signal gating; and
5 control the electronic device to identify one of the segments
6 that is a source of a failure by selectively disabling at least one of the segments; and
7 a computer adapted to employ the test control device to:
8 partition the electronic device into segments by using clock
9 gating or signal gating; and
10 identify one of the segments that is a source of a failure by
11 selectively disabling at least one of the segments.